

J033 U.S. PTO
09/964211



324	158.1
Class	Subclass
ISSUE CLASSIFICATION	

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PATENT NUMBER

U.S. UTILITY Patent Application

O.I.P.E.	PATENT DATE
SCANNED _____ Q.A. _____	

APPLICATION NO. 09/964211	CONT/PRIOR D F	CLASS 324	SUBCLASS 158.1	ART UNIT 2133	EXAMINER J. KER VEROS
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APPLICANTS

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TITLE

Semiconductor device testing apparatus and a test tray for use in the testing apparatus

PTO-2040
12/99

ISSUING CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)						
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					
324	158.1							
INTERNATIONAL CLASSIFICATION								
B65G	43/00							

☐ Continued on Issue Slip Inside File Jacket

<input checked="" type="checkbox"/> TERMINAL DISCLAIMER 09/964,211 <input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed. <input checked="" type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S. Patent. No. 6,459,259 <input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.	DRAWINGS Sheets Drwg. 14 Figs. Drwg. 21 Print Fig. 1 JAMES KER VEROS (Assistant Examiner) 11/2/01 (Date)			CLAIMS ALLOWED Total Claims 87 Print Claim for O.G. 1 NOTICE OF ALLOWANCE MAILED ISSUE FEE Amount Due _____ Date Paid _____ ISSUE BATCH NUMBER	
	(Primary Examiner) _____ (Date) _____ (Legal Instruments Examiner) _____ (Date) _____				

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